

PATENT ABSTRACTS OF JAPAN

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(21)Application number : 02-140386 (71)Applicant : NEC CORP

(22)Date of filing : 30.05.1990 (72)Inventor : USUKI SHIGERU

(54) RE-TIMING CIRCUIT

(57)Abstract:

PURPOSE: To attain pulse delete processing or pulse addition processing effectively by adjusting a change timing by a timing adjustment means when the result of detection of a phase difference shows the same consecutive codes for the prescribed number of times.

CONSTITUTION: A counter 12 counts the number of times of consecutive '+' or '-' and a comparator circuit 13 compares the count with a predetermined reference value. When the number of times of the same code state of a phase difference reaches a reference value, a pulse width signal is outputted from the comparator circuit 13 and inputted to a weighting circuit 11. That it, the counter 12 and the comparator circuit 13 are provided to apply weighting when the same code state of the internal timing, the reception data and the phase difference is consecutive for the prescribed number of times of over, that is, the phase between the internal timing and the reception data is deviated. Thus, the pulse delete processing or pulse addition processing are quickly implemented.

